a distributed bragg reflector mirror epitaxially grown upon a semiinsulating GaAs substrate;

a first layer of P+ type GaAs deposited on said epitaxial mirror;

a layer of P+ type aluminum gallium arsenide ((70%Al) disposed on said layer of GaAs;

a layer of P type aluminum gallium arsenide ((70%Al) disposed on said layer of P+ type aluminum gallium arsenide;

a [PHEMT] Pseudomorphic High Electron Mobility Transistor (PHEMT) transistor epitaxial layer structure without a schottky contact and using N

type modulation doping, disposed on said layer of P type aluminum gallium arsenide, said PHEMT epitaxial layer structure comprising a layer of aluminum gallium arsenide ((15%Al), a layer of GaAs, one to three quantum wells of strained InGaAs separated by GaAs barriers, a spacer layer of aluminum gallium arsenide ((15%Al), a modulation doped layer of aluminum gallium arsenide ((15%Al) and a gate spacer layer of aluminum gallium arsenide ((15%Al) ;

a planar doped layer of P+ type aluminum gallium arsenide ((15%Al) disposed on said PHEMT epitaxial layer structure;

a cladding layer of aluminum gallium arsenide ((70%Al) of modest P type doping disposed on said planar doped layer;

a layer of GaAs of P++ type doping disposed on said cladding layer.

2.A charge coupled device (CCD) realized with the epitaxial growth structure as described in claim 1, comprising a linear array of mesas in which charge may be stored and transferred from one mesa to the next by a suitable arrangement of clock pulses applied to said mesas, said linear array being terminated in a charge sensitive amplifier

for the purposes of detection of said stored charge when transferred to said amplifier, said mesas being adjacent to each other and separated by transfer regions which have been etched from the original surface to the top of a lower P+ planar-doped layer, said transfer regions being implanted with N+ type doping to form a low resistance path between said mesas thereby enabling high efficiency transfer; each pixel being comprised of a barrier section and a storage section, said barrier section being defined by a refractory metal top electrode which results in an enhancement transistor threshold in said barrier regions, and said barrier region being connected electrically by an uppermost p+ charge sheet to said storage region to maintain an equipotential across said mesa, said storage region forming an optical aperture with no metal top contact and being shifted electrically in threshold by an ion implant resulting in a depletion transistor in said storage region, said storage region being contained in a vertical optical cavity, said cavity being terminated in the vertical direction on its top surface by a deposited DBR mirror and on its bottom by a grown epitaxial mirror so that resonant absorption may occur in said cavity formed by said mirrors for light admitted to the structure from either the top or the bottom of said cavity.

3.A device as described in claim 2 wherein only a single pixel is associated with each output charge detection and amplification stage, a configuration defined as an active pixel structure, having the advantage over a CCD of a minimum loss corresponding to a single transfer to an dedicated output charge sensitive amplifier to that pixel and having the disadvantage of a larger area per pixel resulting from said dedicated amplifier.

4.A CCD as described in claim 2 wherein every other pixel is baised to a constant voltage and the remaining pixels are clocked with a single phase clock to produce 1 ½ phase operation.

5.A CCD as described in claim 2 wherein every other pixel is clocked with a phase I clock and the remaining pixels are clocked with a phase II clock to produce 2 phase operation.

6.A CCD as described in claim 2 wherein every third pixel is clocked with a phase I clock, the adjacent pixels to every third pixel are clocked with a phase II clock and the remaining pixels are clocked with a phase III clock to produce 3 phase operation.

7.A CCD as described in claim wherein implants are placed strategically to obtain uniphase operation

8.A CCD as described in claim 2 wherein the quantum well absorbs input radiation by an intersubband absorption mechanism and wherein said absorption is enhanced by the resonance of a cavity containing said storage region, said input radiation causing electrons residing in a substantially populated well to be emitted from a bound quantum well state into a quasi-bound state at the top of said quantum well or into a continuum of states energetically above said quantum well and to be conducted by thermionic emission, drift and diffusion processes into a gate capacitor section positioned immediately above said quantum well, said emitted electrons producing a deficiency of electrons in said quantum well, said deficiency representing a disturbance from thermal equilibrium which can only be restored by the addition of electrons to said well via the thermal generation of electrons across the bandgap of the host material which is large enough to inhibit dark current flow to such small levels that background limited operation